Microcontrol and Arithmetic Units

The introduction of the Signetics Bit-Slice Microprocessors has brought new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar microprocessors with industry standard memory and support circuits, microinstruction cycle times of 100ns are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics slice microprocessors has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Furthermore, systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

Typically, slice microprocessors are employed in the realization of the Central Processing Unit (CPU) of a computer or for implementing dedicated smart controllers. The generalized and simplified structure of a CPU or "Smart" controller can be typically classified into 3 distinct but interactively related functional sections. These sections are generally referred to as the Processing section, the Control section, and the I/O and Memory Interface section. A simplified block diagram of a CPU is illustrated in Figure 1.

The major functions of the Processing section are to:

- provide data transfer paths;
- manipulate data through logic and arithmetic operations;
- provide storage facilities such as a register file; and
- generate necessary status flags based on the kind of operation performed by the ALU.

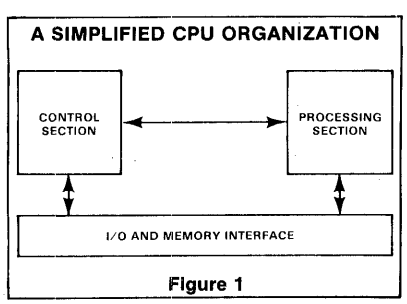


Figure 1

The major functions of the Control section are to:

- initiate memory or I/O operations;
- decode macroinstructions;
- control the manipulation and transfer of data;
- test status conditions; and
- sample and respond to interrupts.

The major functions of the I/O and Memory Interface section are to:

- multiplex data to the proper destination;
- provide bus driving/receiving capability; and
- provide latching capability.

With state-of-the-art bipolar Schottky technology, high-performance microprocessors are designed to perform functions of the Processing section. Due to the limitation on the number of pins and chip size, the overall Processing section is partitioned into several functionally equivalent slices. In today's bipolar microprocessor market, 2-bit and 4-bit slice architecture predominates. Each architecture type has its uniqueness but, in general, a slice contains a group of general purpose registers, an accumulator, special-purpose register(s) ALU and related status flags. All of these elements constitute the Processing section of a CPU. The flexibility of slice components allows the designer to construct a processing section of any desired width as required by his application.

The Control section of the CPU is more complex in design. Typically this section includes the macroinstruction decode logic, test-branch decode, microprogram sequencing logic, and the control store where the microprogram resides. Aside from the microprogram, the remaining portion of the Control section (macroinstruction decode and test-branch decode and sequencing logic), does not lend itself to efficient partitioning into vertical slices. This is due to the random nature of the logic usually found in the Control section. However, horizontal functional grouping is possible. For example, the macroinstruction decode and test-branch decode logic can now be replaced by the FPLA (Field Programmable Logic Array); the random logic traditionally needed to implement the microprogram sequencing can now be replaced by the Microprogram Control Unit; and, of course, the microprogram can be stored in high density PROMs or ROMs. Since the designer must define his own microstructure, the slice microprocessors permit fundamental optimizations to be made. With slice hardware, the designer may have no macroinstructions at all, placing all of the program in PROM for dedicated control applications. Or he may define, as required, any number of macroinstructions selected specifically for his particular processor purpose. Various minicomputers and several MOS microprocessors have been emulated using slice hardware.

The I/O and Memory Interface section consists mainly of I/O ports, high power bus drivers, receivers, and some temporary register storage facilities. Bidirectional and tri-state devices are the most popular logic elements for implementing this interface structure.

Figure 2 shows an LSI approach to the implementation of the same generalized CPU structure indicated earlier.

Data specifications for Signetics' line of slice microprocessor components are contained within this chapter. Included is the popular 3000 series Microprogram Control Unit and the 2-bit slice Central Processing Element. These Signetics devices feature improved performance specifications over 3000 series components available on the general market. Moreover, the unique Signetics XL plastic package design results in significantly cooler operation of the chip than was previously possible with other plastic package designs. This section also features the 8X02 Control Store Sequencer. This device may be used with any TTL compatible slice processing elements and features extreme ease of use. The 8 simple, yet powerful, instructions permit subroutining and looping (using internal stack), unrestricted jumping, unrestricted conditional branching and conditional instruction skipping.

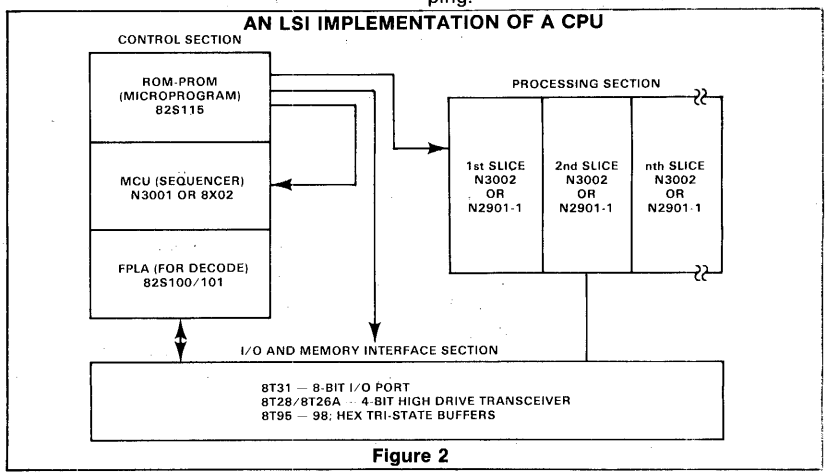


Figure 2

DESCRIPTION

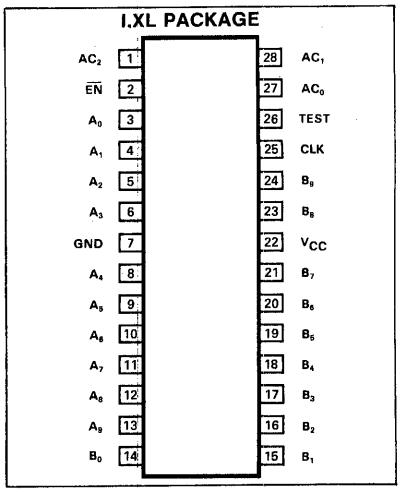
The Signetics 8X02 is a low power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequential logic.

FEATURES

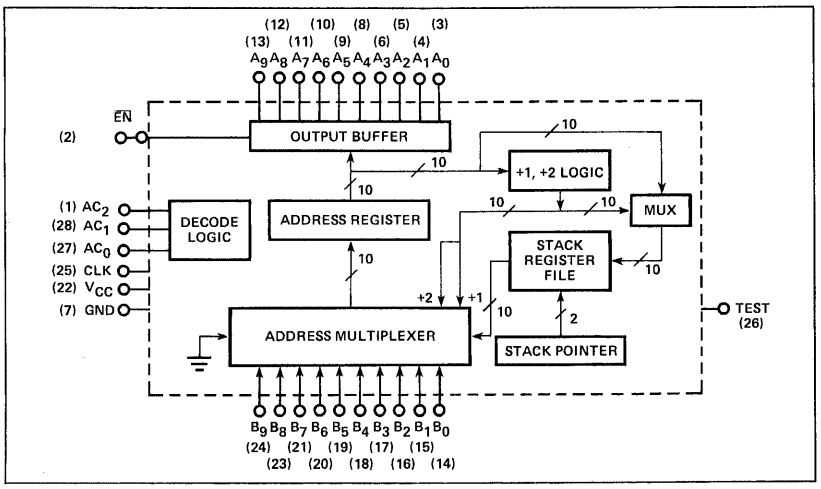
- **Low power Schottky process**
- **1024 microinstruction addressability**
- **N-way branch**
- **4-level stack register file (LIFO type)**
- **Automatic push/pop stack operation**
- **"Test and skip" operation on test input line**
- **3-bit command code**
- **Tri-state buffered outputs**
- **Auto-reset to address 0 during power-up**
- **Conditional branching, pop stack, and push stack**

PIN CONFIGURATION

I,XL PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
5-6 8-13	A_0-A_9	Microprogram Address outputs	Three-state Active high
1,28,27	AC_0-AC_2	Next Address Control Function inputs All addressing control functions are selected by these command lines.	Active high
14-21 23-24	B_0-B_9	Branch Address inputs Determines the next address of an N-way branch when used with the BRANCH TO SUBROUTINE (BSR) or BRANCH ON TEST (BRT) command.	Active high
2	$\overline{EN}$	Enable input When in the low state, the Microprogram Address outputs are enabled.	Active low
25	CLK	Clock Input—High to Low transition for stack operations, Low to High transition for address modification.	⎍
26	TEST	Test input Used in conjunction with four NEXT ADDRESS CONTROL FUNCTION commands to effect conditional skips, branches, and stack operations.	Active high
7	GND	Ground	
22	V_{CC}	+5 Volt supply	

FUNCTIONAL DESCRIPTION

The Signetics 8X02 Control Store Sequencer is an LSI device using low power Schottky technology and is intended for use in high performance microprogrammed applications. When used alone, the 8X02 is capable of addressing up to 1K words of microprogram. This may be expanded to any microprogram size by conventional paging techniques.

The Address Register consists of 10 D-type, edge-triggered flip-flops with a common clock. A new address is entered into the Address Register on the low-to-high transition of the clock. The next address to be entered into the Address Register is supplied via the Address Multiplexer.

The Address Multiplexer is a 5-input device that is used to select either the branch input, +1 adder, +2 adder, stack register file, or ground (all zeros) as the source of the next microinstruction address. The proper multiplexer channel is automatically selected via the Decode Logic according to the Address Control Function Input and Test Input line.

The +1, +2 logic is used to increment the present contents of the Address Register by 1 or 2, depending on the function input command. Thus, the next address to the Control Store ROM/PROM may be either the current address plus 1 (N+1) or the current address plus 2 (N+2). If the same Microprogram Address is to be used on successive occasions, the clock to the 8X02 must simply be disabled; therefore, no new address is loaded into the Address Register.

The Stack File Register is used to provide a return address linkage whenever a subroutine or loop is executed. The 4X10 stack operates in a last-in, first-out (LIFO) mode, with the stack pointer always pointing to the next address to be read. Operation of the stack pointer is automatically controlled by the Address Control Function Inputs. Since the stack is 4 words deep, up to 4 loops and/or subroutines may be nested.

The branch input is a 10-bit field of direct inputs to the multiplexer which can be selected as the next control store address. Using the appropriate branch command, an N-way branch is possible where N is the address of any microinstruction within the 1024 word microcode page. Likewise, the RESET command is a special case of an N-way branch in which the multiplexer selects an all zeros input, forcing the next microinstruction address to be zero.

The Test Input line is used in conjunction with the conditional execution of 4 Address Control Function commands. When the Test Input is false (low), the sequencer simply increments to the next address (N+1). When it is true (high), the sequencer executes a branch as defined by the input command, thereby transferring control to another portion of the microprogram.

All Address Output lines of the 8X02 are three-state buffered outputs with a common enable line ($\overline{EN}$). When the Enable line is high, all outputs are placed in a high-impedance state, and external access to the control store ROM/PROM is possible. This allows a preprogrammed set of microinstructions to be executed from external or built-in test equipment (BITE), vectored interrupts, and Writable Control Store if implemented.

NEXT ADDRESS CONTROL FUNCTION TABLE

MNEMONIC	DESCRIPTION	FUNCTION AC_2 1 0	TEST	NEXT ADDRESS	STACK	STACK POINTER
TSK	Test and skip	0 0 0	False True	Current + 1 Current + 2	N.C. N.C.	N.C. N.C.
INC	Increment	0 0 1	X	Current + 1	N.C.	N.C.
BLT	Branch to loop if test input true	0 1 0	False True	Current + 1 Stack reg file	X POP (read)	Decr Decr
POP	POP stack	0 1 1	X	Stack reg file	POP (read)	Decr
BSR	Branch to subroutine if test input true	1 0 0	False True	Current + 1 Branch address	N.C. PUSH (Curr + 1)	N.C. Incr
PLP	Push for looping	1 0 1	X	Current + 1	PUSH (Curr Addr)	Incr
BRT	Branch if test input true	1 1 0	False True	Current + 1 Branch address	N.C. N.C.	N.C. N.C.
RST	Set microprogram address output to zero	1 1 1	X	All O's	N.C.	N.C.

X = Don't care
N.C. = No change

FUNCTIONAL DESCRIPTION

The following is a description of each of the eight Next Address Control Functions (AC_2-AC_0)

MNEMONIC	FUNCTION DESCRIPTION
TSK	AC_{2-0} = 000: TEST AND SKIP Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Current Address + 2 (i.e. Skip next microinstruction) Stack Pointer unchanged
INC	AC_{2-0} = 001: INCREMENT Next Address = Current Address + 1 Stack Pointer unchanged
BLT	AC_{2-0} = -010: BRANCH TO LOOP IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer decremented by 1 If test is True (High): Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
POP	AC_{2-0} = 011: POP STACK Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
BSR	AC_{2-0} = 100: BRANCH TO SUBROUTINE IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer incremented by 1 PUSH (write) Current Address + 1 → Stack Register File
PLP	AC_{2-0} = 101: PUSH FOR LOOPING Next Address = Current Address + 1 Stack Pointer incremented by 1 PUSH (write) Current Address → Stack Register File
BRT	AC_{2-0} = 110: BRANCH ON TEST CONDITION TRUE Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer unchanged
RST	AC_{2-0} = 111: RESET TO ZERO Next Address = 0 Stack Pointer unchanged

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-State output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°	°C

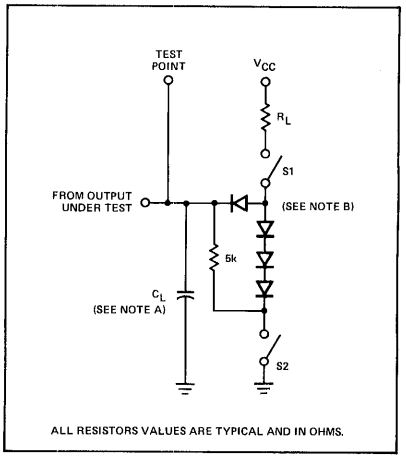
DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, $4.75 \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = -2.6mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 4.75V, I_{OL} = 8mA			0.5	V
I_I	Input current at maximum Input voltage	V_{CC} = 5.25V, V_I = 5.5V			100	μA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	AC_2-AC_0, $\overline{EN}$, TEST				40	μA
	B_9-B_0				20	μA
	CLK				60	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.4V				
	AC_2-AC_0, $\overline{EN}$, TEST				-0.72	mA
	B_9-B_0				-0.36	mA
	CLK				-1.08	mA
I_{OS}	Short-circuit output current	V_{CC} = 5.25V	-15		-100	mA
I_{OZH}	High-Z state output current	V_{OUT} = 2.7V			20	μA
I_{OZL}	High-Z state output current	V_{OUT} = 0.4V			-20	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	200	mA

NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.

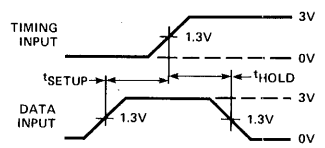
TEST LOAD CIRCUIT



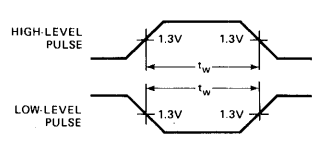
NOTES
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. R_L = 2k, C = 15pF.

VOLTAGE WAVEFORMS

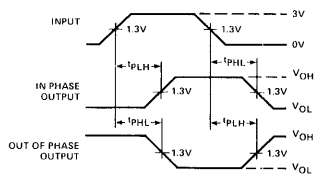
SETUP AND HOLD TIMES



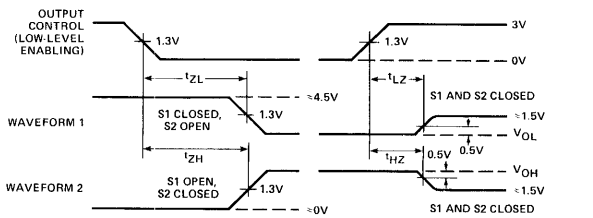
PULSE WIDTHS



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



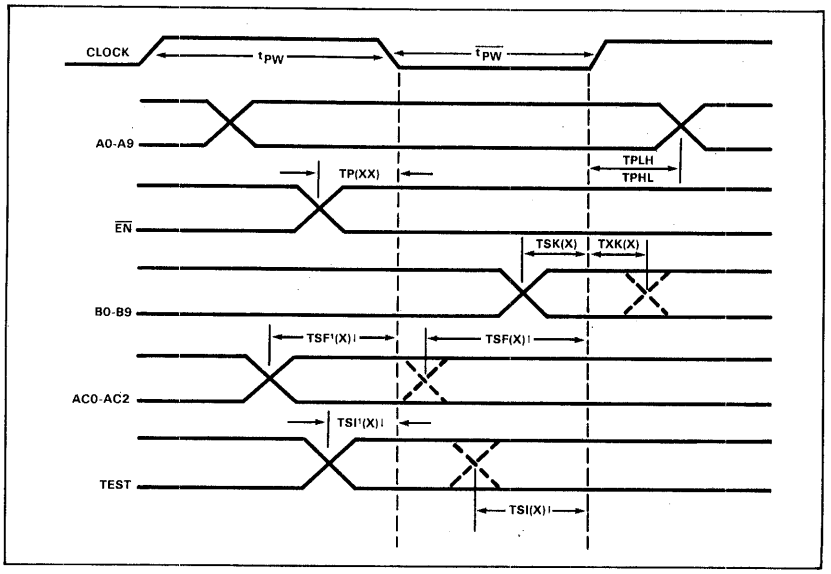
AC ELECTRICAL CHARACTERISTICS T_A = 0° -70°C, V_{CC} = 5.0V ± 5%

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
t_{HI} (1)	Test			0	-10		ns
(0)				0	-24		
	Control and data input setup times with respect to CLK (↓) for stack related functions (BLT, POP, BSR, PLP) (2)						ns
t_{SF}[1] (1)	AC_0-AC_2			35	23		
(0)				35	22		
t_{SI}[1] (1)	Test			28	23		
(0)				28	22		
	Propagation delay	A_0-A_9	EN				ns
t_{PLZ}	Low to high Z				12	35	
t_{PHZ}	High to high Z				16	35	
t_{PZL}	High to low				14	25	
t_{PZH}	High Z to high				15	35	
	Propagation delay	A_0-A_9	Clock				
t_{PHL}	High to low				33	40	
t_{PLH}	Low to high				33	40	
	Clock pulse width						ns
t_{PW}	High			50	36		
t_{PW}	Low			60	42		
	Control and data input setup times with respect to CLK (↓) for non-stack related functions (TSK, INC, BRT, RST)						ns
t_{SF} (1)	AC_0-AC_2			90	70		
(0)				90	70		
t_{SK} (1)	B_0-B_9[2]			27	22		
(0)				29	24		
t_{SI} (1)	Test			60	45		
(0)				60	45		
	Control and data input hold times with respect to CLK (↓)						ns
t_{HF} (1)	AC_0-AC_2			0	-7		
(0)				0	-12		
t_{HK} (1)	B_0-B_9[2]			0	-12		
(0)				0	-10		

NOTES

1. Typical values are to T_A = 25°C and V_{CC} = 5.0 volts
2. B_0-B_9 inputs are required to Clock (↓) only. See TSK (1) and TSK (0).

TIMING WAVEFORM



PULSE WIDTH ($\overline{TPW}$) vs TEMPERATURE